Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-3. (Canceled)

4. (Currently Amended) ~~The digital circuit according to claim3, characterized in that~~ A digital circuit comprising:

a delay circuit that provides variable timing of a clock signal;

a delay amount of the delay circuit;

a delay synchronizing loop that stabilizes the delay amount; and

a delay amount setting voltage generating circuit that synthesizes two or more reference voltages,

wherein the delay amount setting voltage generating circuit synthesizes ~~reference~~ the reference voltages ~~by means of~~ based on a piece-wise linear approximation.

5. (Currently Amended) ~~The digital circuit according to claim 3, characterized in that~~ A digital circuit comprising:

a delay circuit that provides variable timing of a clock signal;

a delay amount of the delay circuit;

a delay synchronizing loop that stabilizes the delay amount; and

a delay amount setting voltage generating circuit that synthesizes two or more reference voltages,

wherein the delay amount setting voltage generating circuit is a voltage dividing type circuit.

6. (Currently Amended) ~~The digital circuit according to claim 3, characterized in that~~ A digital circuit comprising:

a delay circuit that provides variable timing of a clock signal;

a delay amount of the delay circuit;

a delay synchronizing loop that stabilizes the delay amount; and

a delay amount setting voltage generating circuit that synthesizes two or more reference voltages,

wherein the delay amount setting voltage generating circuit is a ladder type circuit.

7-9. (Canceled)